Signal Integrity

Signal retains integrity in that TPS signals are processed entirely through analog circuitry and therefore do not undergo any resolution losses that come with ADC processing. Circuit designed in such a way that output of amplifiers doesn’t clip through use rail-to-rail outputs.

APPS Fault and Plausibility Checks

The APPS performs two plausibility checks on each scaled TPS signal to check for faults in the sensors. The board also performs a check to see if the brakes are actuated whilst the pedal is past a certain travel (EV.2.4).

Boundary

Two potentiometers are used to configure the maximum (Vmax) and minimum (Vmin) expected voltage levels for 100% and 0% travel respectively. A series of comparators are then used to check each signal against these boundaries. If either signal is out of bounds (from a TPS short circuit

for eg) then a fault condition occurs.

Tolerance

The tolerance circuit checks that each TPS signal agrees within 10% pedal travel. The voltage

corresponding to 10% travel is found through a differential amplifier circuit which subtracts

Vmin (0% travel) from Vmax (100% travel) and scales the output by 1/10. A series of differential

amplifier and comparator circuits are then used to check if TPS1 - TPS2 is less than the tolerance

value and vice-versa. If the difference is above the tolerance, then a fault condition occurs.

Pedal Position

A latching circuit is used to enter a fault state if the accelerator pedal is past 25% travel whilst the brakes are active (signal from brake switch). This fault condition remains active until the accelerator pedal is below 5% travel

Fault Output

Should a boundary or Tolerance fault occur for more than 100ms then the circuit will ground the output of the APPS through use of an analog switch. The pedal position fault grounds the APPS through the same switch however it bypasses 100ms delay.